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Design of the Low Noise Amplifier Circuit in Band L for Improve the Gain and Circuit Stability

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Abstract

In this paper, focuses on the design of Low Noise Amplifier circuitry in the frequency band L. This circuit is designed using the 0.18 nm CMOS transistor technology, which consists of two transistor Stage. The purpose of this research is to improve the cost of: Increase Gain - Increase circuit linearization - Create an integrative matching network for system stability. The application of this circuit can be used in wireless and GPS systems. The CMOS LNA exhibits a gain greater than 23 dB from 1.1 to 2.0 GHz, and a noise figure of 2.7 to 3.3 dB from 1.2 to 2.4 GHz. At 1.575 GHz, the 1-dB compression point (P1dB) is 1.73 dBm, with an input third-order intercept point (IIP3) of -3.98 dBm. This circuit is designed using ADS software.

Keywords:

Gain;
Noise Figure;
LNA;
Linearization;
L Band.

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1- Introduction

Built-in Global Positioning System (GPS) capability is increasingly becoming a standard feature for cellular handset and other low-cost embedded applications. The requirements for these systems provide a strong motivation for developing highly integrated and low-cost GPS receivers. Low-noise amplifiers (LNAs) in GPS receivers are often the most challenging block to implement, given the difficulty of simultaneously achieving sufficient gain, low noise figure, and low power consumption. Typically, GPS receivers operate in the L-band frequency range (1575.42 MHz (L1), 1227.60 MHz (L2), 1381.05 MHz (L3) and 1176.45 MHz (L5)). Designing a monolithic LNA at L-band poses significant challenges due to the large size of the passive components, making it difficult to implement the LNA with its requisite matching networks on-die. Complementary Metal-Oxide-Semiconductor (CMOS) [1] are attractive for analog, mixed-signal and RF applications because they exhibit very low noise figure and very high power gain, at modest power dissipation levels, which can be leveraged to improve the sensitivity of receiver front-ends. CMOS technology utilizes band gap engineering to improve transistor performance, and at present peak cutoff frequency (fT) and peak maximum oscillation frequency (fmax) greater than 300 GHz have been achieved at modest lithographic feature size (0.18 nm), while maintaining compatibility with the traditional CMOS processes In this paper, we present a high gain, L-band CMOS LNA with fully-integrated on-chip matching networks. At 1.575 GHz, the LNA achieves a gain of 26 dB, a NF of 3.2 dB, while dissipating 17.89 mW of dc power.

Communication systems have been improving a lot in the last decades [1]. An important factor determining their improvement is on RF front end circuits [4, 6, 8, 9]. RF front-end components with high linearity and flat gain performance as well as high efficiency and low thermal dissipation loss are highly necessary [2, 3, 5, 7]. In case of satellite telecommunication, signal transmission travelling thousands of miles from the ground station-to-satellite and satellite-to-receiving fixed and mobile stations demands RF front-end transistors meeting stringent requirements. Specifications, including the low noise amplifier of receiving section. The low noise amplifier of the front-end should have sufficient sensitivity to receive very low signal amplitude as result through long distance propagation from satellite

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at the orbital altitude to the terminal at the ground. As receiving section of the front end is sensing very low magnitude signal transmitted from satellite transponder, the Low Noise Amplifier (LNA) transistor plays the most important role in receiver front end circuit. The transistor used in this paper's LNA design is BFP720ESD, a Silicon Germanium Carbon (CMOS:C) NPN Hetero junction, a wideband RF Transistor [10]. This CMOS shows very low noise figure and low power consumption meeting ideal condition for an LNA implementation. The CMOS LNA has been designed meticulously. Proposed design in this paper shows high gain (35.56dB) with very low noise figure (0.628dB) using this transistor. Modulation analysis has also been performed in this paper to gain EVM (error vector magnitude) and ACLR (adjacent channel rejection ratio) parameters with WCDMA input signal of 3.84 MHz bandwidth [11].

2- LNA Design

The LNA was implemented as a single-ended cascade amplifier [3] with a feedback network. The first stage is a common-emitter (CE) configuration and the second stage is a common-base (CB) configuration. The cascode transistor Q_2 prevents the Miller effect from degrading the power gain and also improves the reverse isolation, and improves stability of the LNA. The feedback topology [5] for the LNA uses a shunt-shunt configuration with both the resistance R_{fb} and the capacitance C_{fb} connected in series. Figure 1 shows the small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascade configuration without feedback. Assuming that the gain at Q_1 is greater Q_2, the equivalent noise input current, I_{ni} for a shunt-shunt feedback amplifier [7] is given as:

$$I_{ni}=\left[\frac{4kT\Delta f}{Rs+f_b}(1+\frac{rx}{R_s+R_{fb}})+2qI_B\Delta f(1+\frac{rx}{R_s+R_b})^2+2qI_c\Delta f\left[\frac{1}{\beta}+\frac{1}{R_s+R_b}\left(\frac{r_x}{\beta}+\frac{V_T}{I_c}\right)\right]^2\right]^{\frac{1}{2}} \quad (1)$$

$$GM=gm \quad (2)$$

$$A_v=gmR_s \quad (3)$$

For the shunt-shunt feedback amplifier, the closed-loop gain A_{close} of the amplifier is given by:

$$A_{close}=\frac{A+\Delta A}{1+(A+\Delta A)B_f}\approx\frac{A}{1+AB_f}+\frac{\Delta A}{1+AB_f} \quad (4)$$

$$A_{close}\approx\frac{1}{B_f}\approx R_{fb} \quad (5)$$

The amount of SNR (in, out) is as follows:

$$SNR_{in}=\int_{-\infty}^{\infty}\frac{|P(\omega)|^2}{SV_g(\omega)}d\omega_0 \quad (6)$$

$$SNR_{out}=\int_{-\infty}^{\infty}\frac{|P(\omega)|^2}{SV_g(\omega)+SV_{in}(\omega)}d\omega_0 \quad (7)$$

The closed-loop input impedance of the feedback amplifier is given by:

$$Z_{if}\approx\frac{R_i(R_{fb})}{R_{fb}+A} \quad (8)$$

Where A is the open-loop gain. The closed-loop output impedance of the feedback amplifier is given by:

$$Z_{of}\approx\frac{R_o(R_{fb})}{R_{fb}+A} \quad (9)$$

The minimum effect of a linear network in the order of the system is expressed in Noise figure. The R_{fb} value is larger than the R_s with the input impedance. Figure 1 shows the small-signal equivalent circuit for the transistors Q_1 and Q_2 in a cascade configuration without feedback. In Figure 2, the schematic of the L-band LNA is shown. Tables 1 shows the device sizes for the LNA.

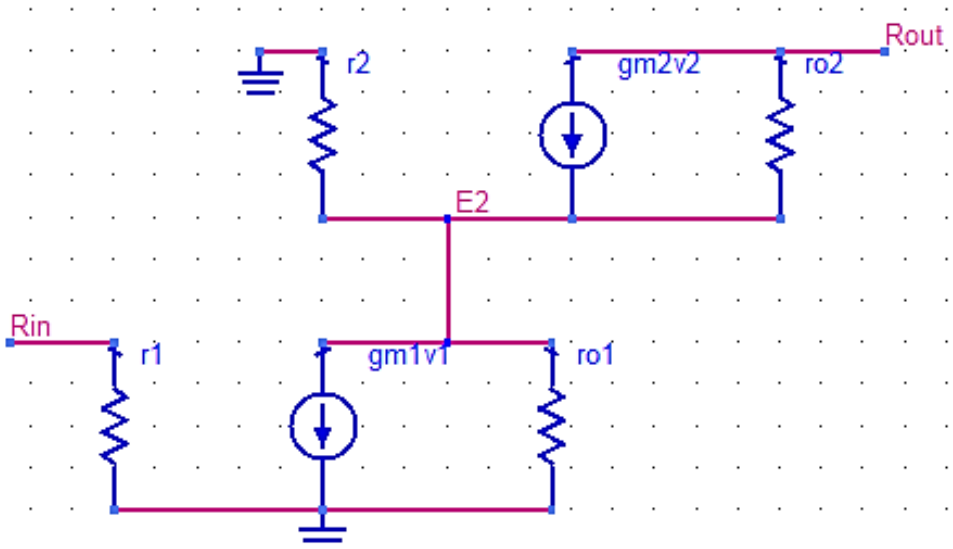

Figure 1. Small-signal.

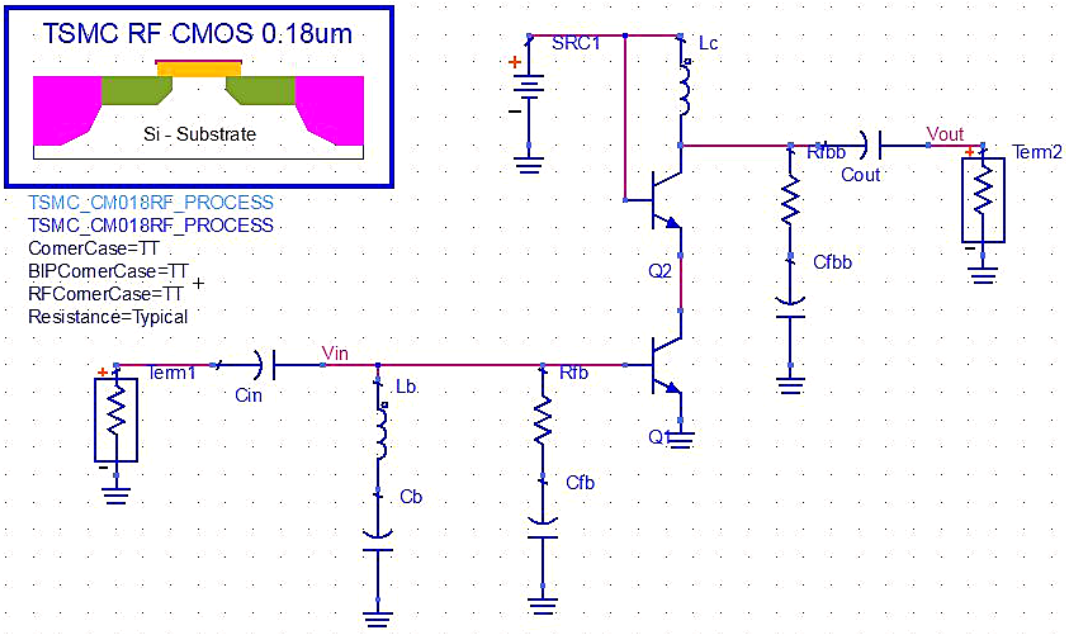

Figure 2. Schematic of the L-band LNA.

Table 1. Device sizes for the L-band CMOS LNA.

Parameter	Q2	Q1	Cout	Cfb	Rfb	Lc	Cb	Lb	Cin
Device Sizes	0.18	0.18	976.8 fF	11.5 KΩ	4.8 KΩ	13.5 nH	10 pF	7.3 nH	2 pF

3- Simulation of LNA

The LNA was designed to operate off of a supply voltage as low as Vcc=1.5 V and Ic=11.9 mA, yielding a total power dissipation of 17.89 mW. The LNA was measured on-wafer using ground-signal-ground (GSG) coplanar microwave probes, with probe-level calibration used to account for cable losses. The LNA achieves a peak gain of 26 dB at 1.575GHz, and from 1.1-4.0 GHz, it maintains a gain above 22 dB. The reverse isolation of the LNA is more than 35 dB from 1 to 4 GHz indicating good stability. The LNA exhibits a good 50 Ω match and Figure 6 shows that the measured and simulated input return loss (S11) and the output return loss (S22) are less than -10 dB from 1.1-1.9 GHz.

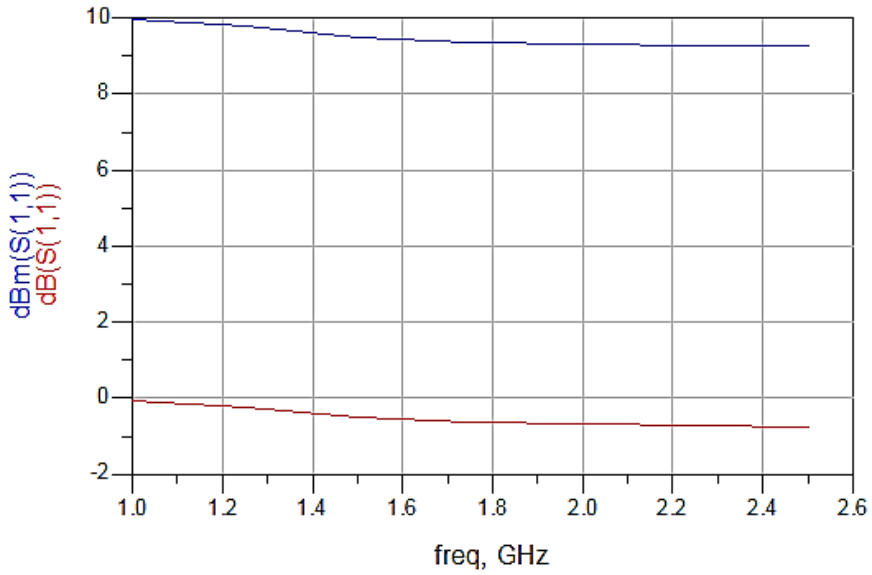

Figure 3. Parameter chart S_{11}.

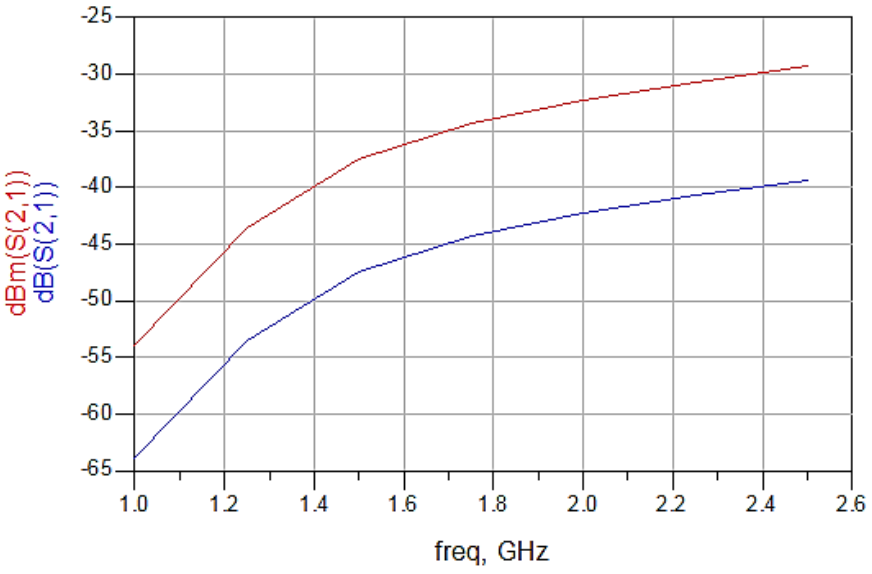

Figure 4. Parameter chart S_{12}.

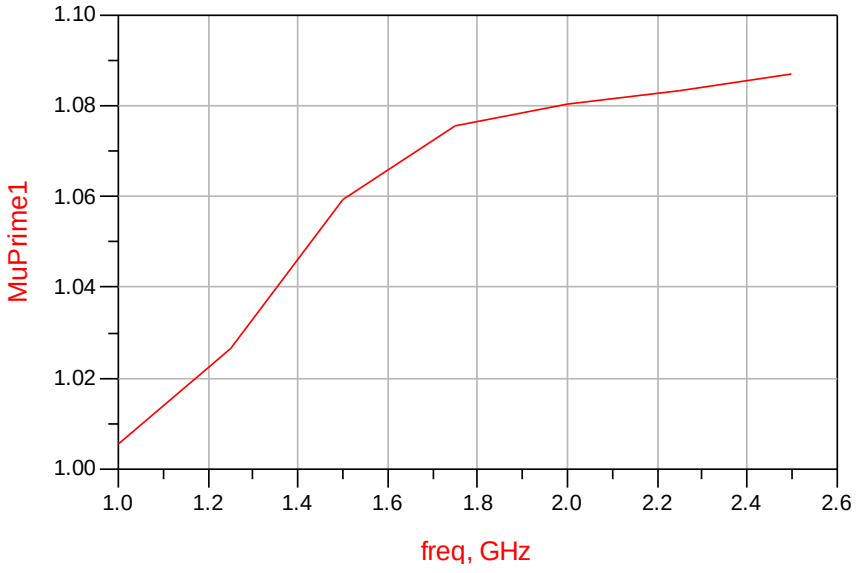

Figure 5. The MU parameter chart of the initial values of S.

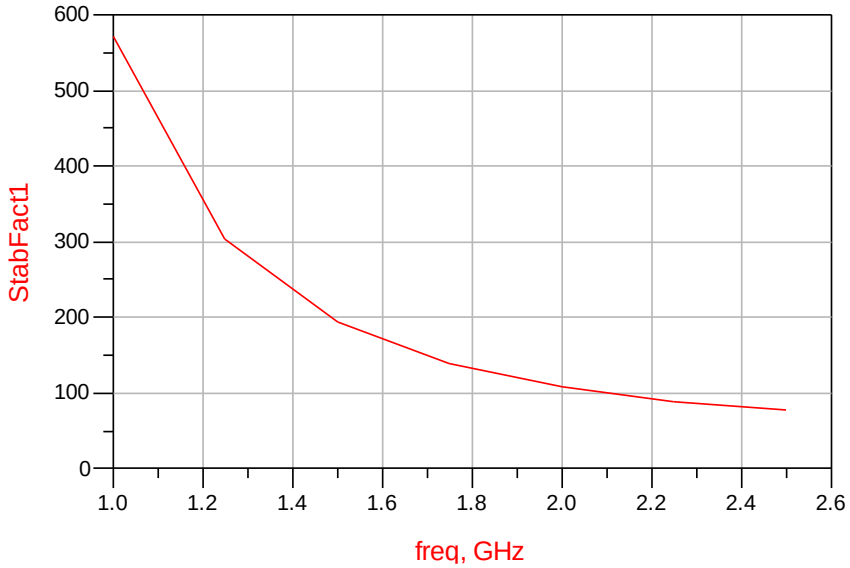

Figure 6. Chart stability.

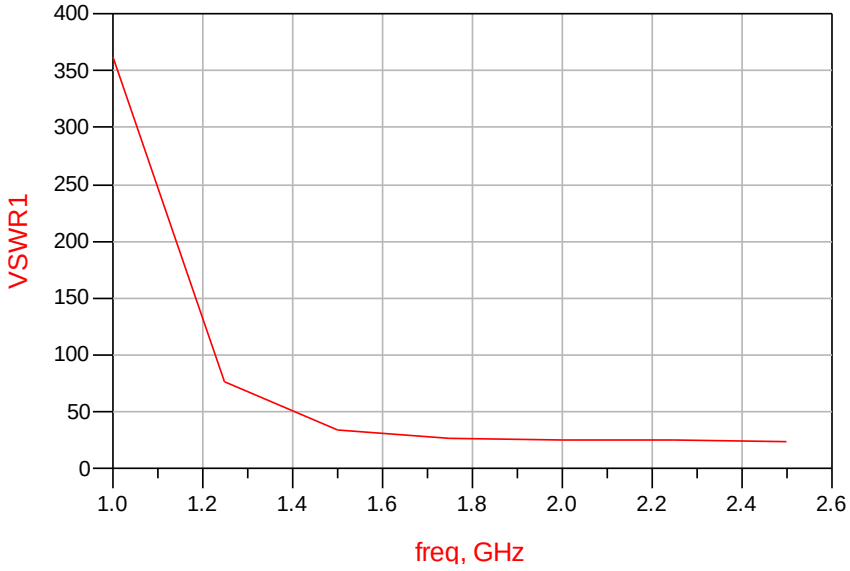

Figure 7. Voltage VSWR chart in parameter S.

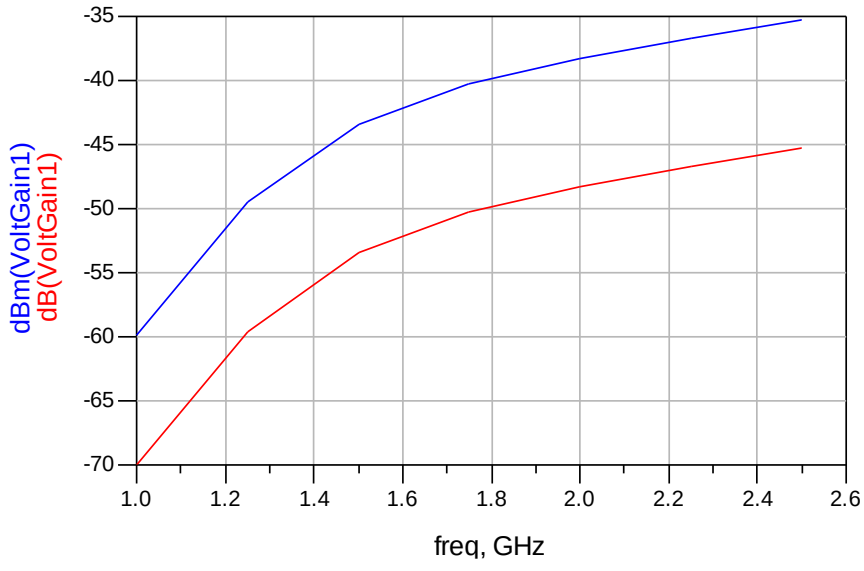

Figure 8. Voltage chart.

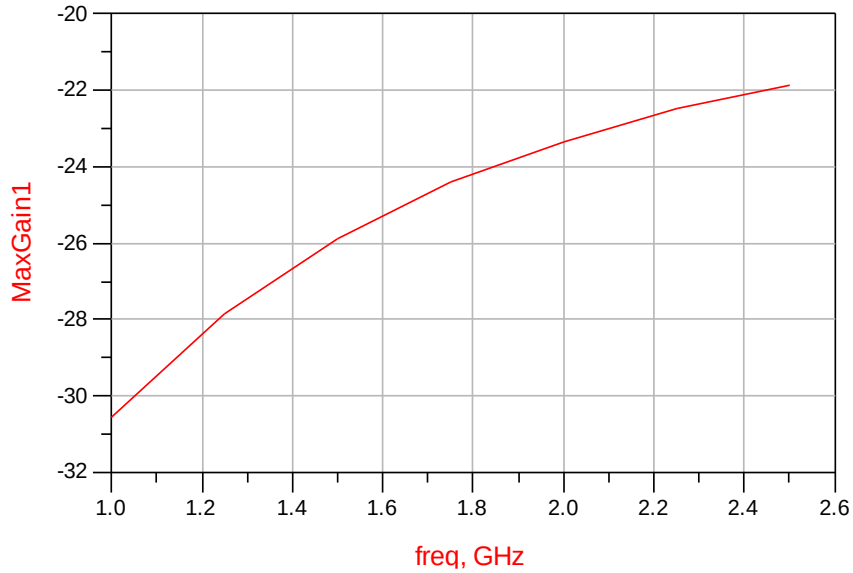

Figure 9. **Maximum Circuit chart.**

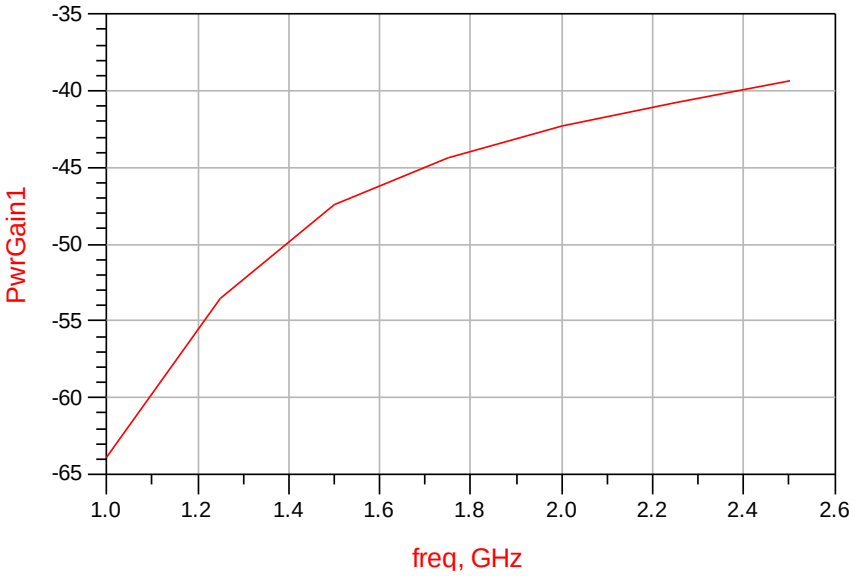

Figure 10. **Circuit output circuit diagram.**

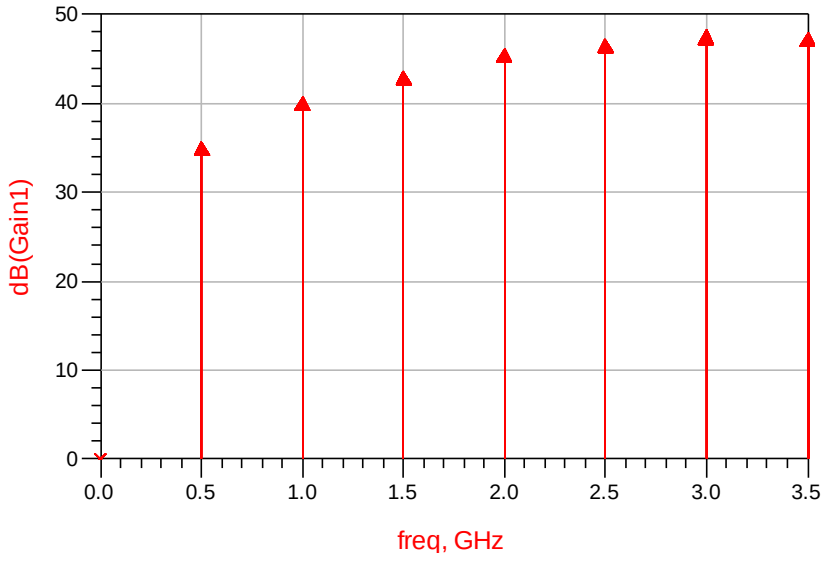

Figure 11. **Gain diagram index.**

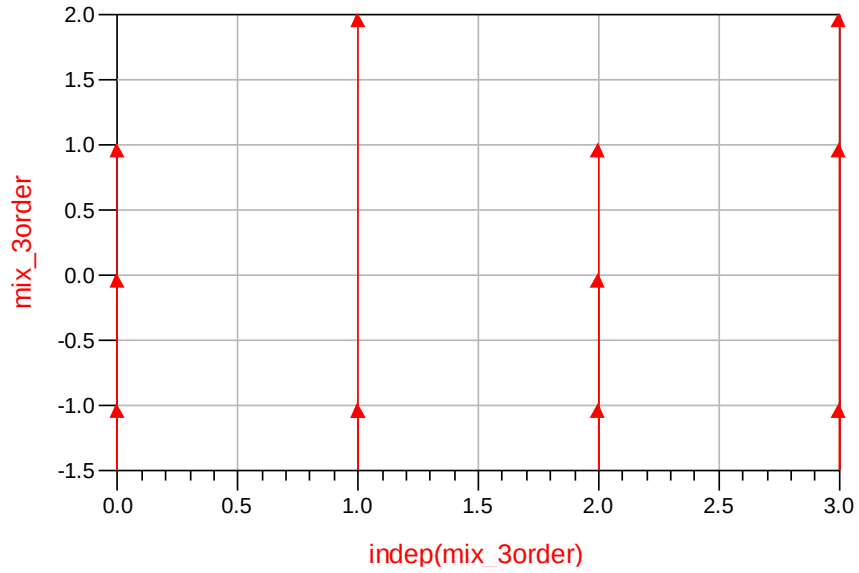

Figure 12. **Harmonic Differential Third-order.**

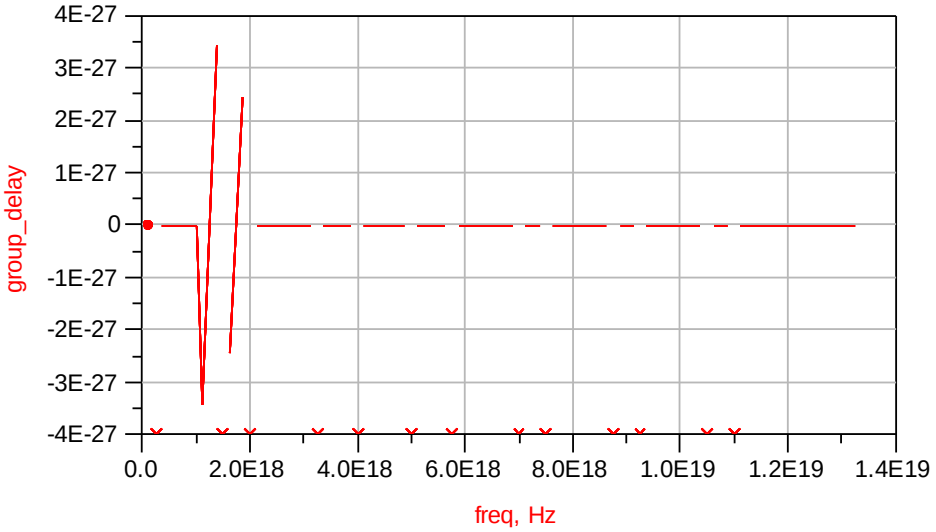

Figure 13. **Characteristic of the harmonic phase harmonic frequency spectrum in terms of frequency.**

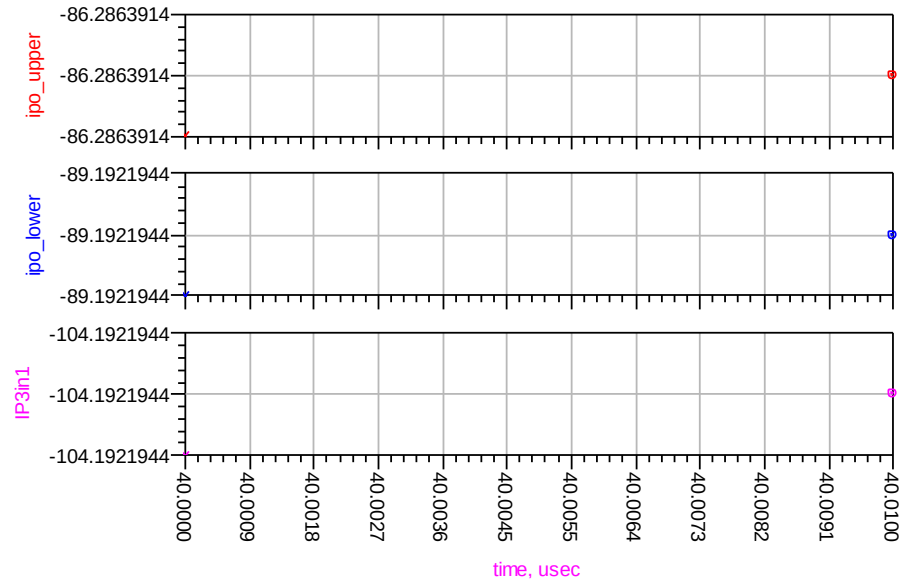

Figure 14. **Chart and IP3 values.**

Table 2 shows that the present LNA has the highest FOM when compared against other L-band LNAs.

$$FOM = \frac{S_{21}(mag).IIP3(mW)}{[NF(mag)-1].P_{diss}(mW)} \quad (10)$$

Table 2. Performance comparison between other l-band low noise amplifiers

FOM	Technology	NF (dB)	VCC (V)	Gain (dB)	Freq (GHZ)	Reference
0.501	0.6 CMOS	2.8	1.5	21	1.5	[1]
0.178	0.8 BiCMOS	2.7	2	10	1.9	[2]
5.381	HBT	2	2	111.1	1.83	[3]
4.631	0.25 CMOS	0.8	1.5	20	1.22	[4]
4.497	0.25 CMOS	1.3	1.5	16.5	1.57	[5]
7.4	0.18 CMOS	2.6	1.5	22.2	1.82	This Work

4- Conclusion

In this paper, we have design and described the LNA circuit in the frequency band L. This circuit is designed with the 0.18 CMOS technology structure. The purpose of this design is to improve the quantity: Gain - Noise Figure - Linearization - Reduced power consumption and circuit stability. This circuit is also used in various wireless systems, including GPS systems and short-range satellite radio frequencies. After designing the circuit, we analyzed the quantities that these quantities were analyzed based on equations or based on the boxes specified in ADS software.

5- Acknowledgement

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