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An Offset-free High linear Low Power High Speed Four-Quadrant MTL Multiplier

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Abstract

In this paper a new CMOS current-mode four-quadrant analog multiplier circuit is proposed. The major advantages of this design are high linearity, high speed and low power consumption. Removing dc offset is the most important improvement in this topology. The circuit is designed with 1.8V supply voltage and is simulated using HSPICE simulator by level 49 parameters in 0.18µm standard CMOS TSMC technology. The aspect ratios of the MOSFETs are optimized using Evolutionary algorithm by MATLAB. The simulation results of this analog multiplier demonstrate a maximum linearity error of 2.6%, a THD of 1.77%, maximum power consumption of 157 µW, -3dB bandwidth of 241MHz and almost free from dc offset.

Keywords:

Current-Mode;
Translinear;
CMOS Analog Multiplier;
Offset Free.

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1- Introduction

Todays, multiplier circuits, especially the four-quadrant ones, are frequently used in such wide range of applications as automatic gain control, phase locked loop, modulation, detection, adaptive filters, square rooting of signals, FPAAs, and neural networks [1, 2]. In all these mentioned application, power consumption plays a major role while, using current-mode technique has proved to highly reduce this major parameter [3, 4].

High speed, low-power, low voltage and well linear multipliers have to be designed by specific structures and technologies. CMOS analog technology is widely recognized as the most desirable technology and method to design this very important block. Several multiplier circuits have been designed using different techniques to reduce power consumption and nonlinearity as the two most important parameters of this circuit. However, they suffer from such problems as low speed and large DC offset. In the multiplier circuits of [2-4] power consumption is very high and the bandwidth is not enough for high speed applications. In [1, 3] the offset error is such considerable that the output is not suitable for high accuracy applications.

2- Structure and Theoretical Analysis of the Proposed Multiplier

The proposed multiplier circuit is shown in Figure1. This circuit is driven by a bias part consisting M_1 and M_2 diode connected MOSFETs that secures V_{SL} as the bias voltage of main part of the circuit. Alternatively, V_{SL} (also V_{GG}) can be provided by V_{DD} through a suitable divided resistor network. Current sources of (x-y) and (x+y) are the input signals of this circuit and I_{Ofo} and I_{Ofi} are the current sources to cancel the offset errors as will be further discussed later. One of the most important nonidealities of the Mos transistors that mainly causes current errors and nonlinearity in current mirror blocks is channel modulation problem. It is regularly produced by either unequal V_{DS} of basic pair transistors of the current mirror (i.e. M_{4A}-M_{5A}, M_{4B}-M_{5B} and the like here) or/and low output impedance of the current mirror. To guarantee both above-mentioned privileges to sustain, transistors M_{3A}, M_{6A}, M_{14}, M_{6B} ,M_{3B} in bottom half and the likes in top half of the multiplier are inserted. In addition, high swing low voltage cascode current mirrors are used to further

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increase the dynamic range and reduce the distortion of the proposed circuit. Thus elaborately realizing all above explained plans has greatly secured the less current error and nonlinearity of the proposed multiplier.

Now assuming all transistors of this structure are well matched, working in saturation region and have the same trasconductance parameters, then applying MTL translinear principle to both traslinear loops of M1, M2, M_{3A}, $M_{4A}$and M1, M2, M_{3B}, M_{4B} in saturation region [5] gives:

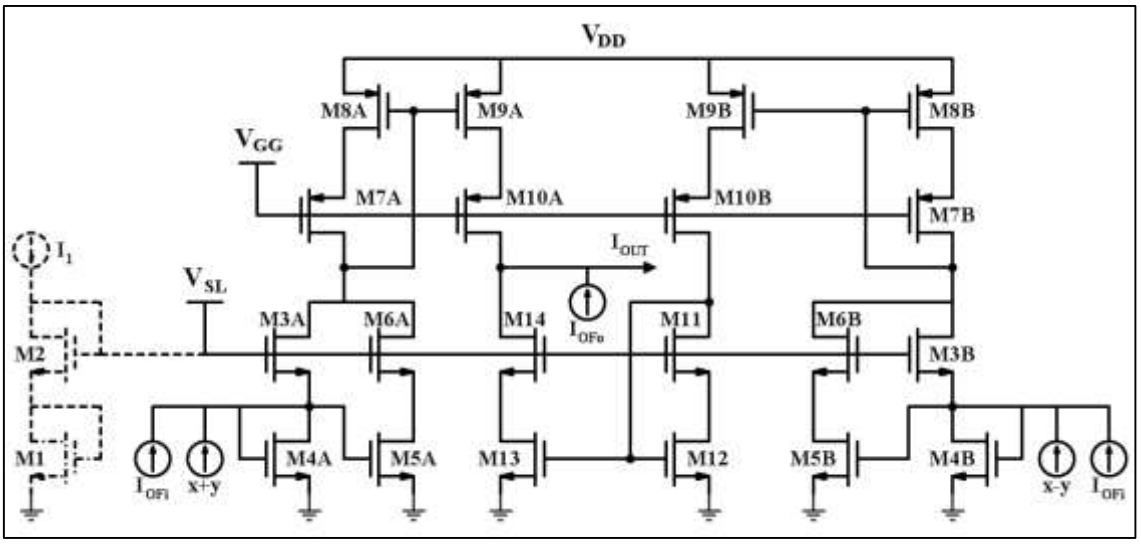

Figure 1. Proposed current-mode analog multiplier circuit

$$2\sqrt{I_1} = \sqrt{I_{3A}} + \sqrt{I_{4A}} \tag{1-A}$$

$$2\sqrt{I_1} = \sqrt{I_{3B}} + \sqrt{I_{4B}} \tag{1-B}$$

By applying KCL at the input and output nodes :

$$I_{4A} = I_{3A} + x + y \tag{2-A}$$

$$I_{4B} = I_{3B} + x - y \tag{2-B}$$

$$I_{OUT} = I_{10A} - I_{14} \tag{3}$$

On the other hand:

$$I_{6A} = I_{5A} = I_{4A} = I_{3A} + x + y \tag{4-A}$$

$$I_{6B} = I_{5B} = I_{4B} = I_{3B} + x - y \tag{4-B}$$

Then to relate output current to input ones and bias current of I1, Equation 3. is expanded as:

$$\begin{aligned} I_{14} &= I_{12} = I_{M10B} = I_{M7B} = I_{6B} + I_{3B} = 2I_{3B} + x - y \\ I_{10A} &= I_{M7A} = I_{6A} + I_{3A} = 2I_{3A} + x + y \end{aligned} \tag{3-A}$$

$$I_{OUT} = (I_{3A} + I_{6A}) - (I_{3B} + I_{6B}) = 2I_{3A} - 2I_{3B} + 2y \tag{3-B}$$

Substituting (2-A) in (1-A) and squaring both sides gives:

$$4I_1 - 2I_{3A} - (x + y) = 2\sqrt{I_{3A}(I_{3A} + x + y)} \tag{5}$$

Then Squaring (5) and simplify the result yields:

$$I_{3A} = \frac{(4I_1 - (x + y))^2}{16I_1} \tag{6-A}$$

Similarly I_{3B} can be extracted as:

$$I_{3B} = \frac{(4I_1 - (x-y))^2}{16I_1} \tag{6-B}$$

Substituting (6-A) , (6-B) in (3-B) produces:

$$I_{OUT} = (\frac{(4I_1 - (x+y))^2}{8I_1} + (x+y)) - (\frac{(4I_1 - (x-y))^2}{8I_1} \tag{7}$$

$$+(x-y))$$

$$\Rightarrow I_{OUT} = \frac{xy}{2I_1} \tag{8}$$

Equation 8. illustrates that the proposed circuit can either be used as a divider by changing (I_1) to a variable parameter or as a multiplier otherwise. In Some applications where there is no need for division, the bias circuit can be replaced by dc voltage source V_{SL} . Equation 9. illustrates that changing the voltage of V_{SL} affects the output current slope; so, the slope of the output current would be voltage controlled. However, current controling of the output current can either be achieved by variation of I_1 current source.

$$I_{OUT} = \frac{xy}{\mu C_{OX} \frac{W}{L} (\frac{V_{SL}}{2} - V_{th})^2} \tag{9}$$

The mismatch between NMOS and PMOS transistors and even between the same type of transistors effect of V_{DS} on drain current plus imbalance between pathes fom input to output cause unexpected phenomena such as offset. Offset can change the circuit's output response and is one of the significant source of error in the circuit. As it is shown in Figure.2, the crossing point is not exactly on zero and the more is the deviation of this crossing point from zero the larger would be the offset value. This offset consists of two components. To cancel this unwanted phenomena, two offset currents of I_{Ofi} and I_{OFo} are applied to the proposed circuit as is shown Figure 1. These offset currents affect the offset of the circuit by changing the current coming to the input and output nodes. Changing the input node's current by I_{Ofi} reduces horizontal offset and change the current in the output by I_{OFo} decreases vertical offset.In practice, these compensating offset values should be applied off chip to the same shown points by proper tunable intermediate current sources. The simpelest tuneable current source which can generate offset currents is shown in Figure 3. in which, by changing POT_{ref} as a tunable resistance, the output current can be changed.

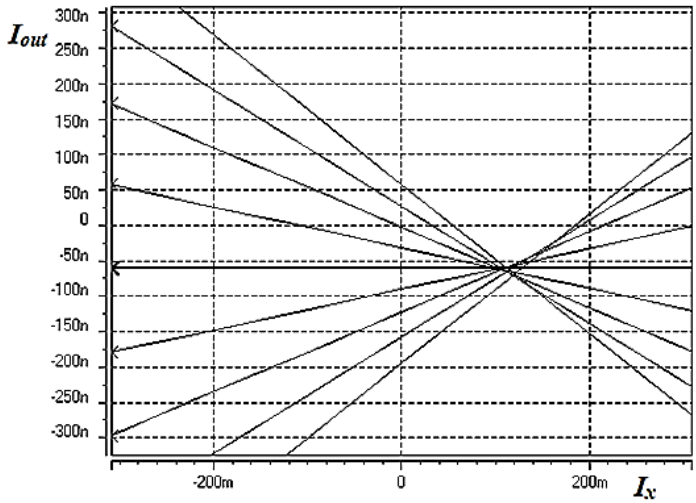

Figure 2. Simulated DC transfer characteristics (Iy is used as sweep parameter)

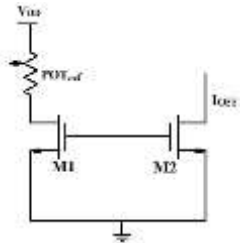

Figure 3. Simplest tunable current source for generating

3- Simulation Results

To verify the performance of the proposed circuit of Figure1. HSPICE is used to simulate the proposed circuit using level 49 parameters in 0.18 *um* standard CMOS TSMC technology and 1.8V supply voltage.the aspect ratios of MOS transistors are listed in table.1 the values of which are optimized by such evelotionary algorithm as is described in [6]. The bias values of the circuit are also given in Table 2.

Table 1. Aspect Ratio of Figure 1. MOSFETs in micrometer

M_{3A}, M_{4A}, M_{5A}, M_{3B}, M_{4B}, M_{5B}	5.4/0.54
M_{9A}, M_{10A}, M_{9B}, M_{10B}, M_{13}, M_{14}	18/0.18
M_{11}, M_{12}	10/0.54
M_{6A}, M_{6B}	26/0.18
M_{7A}, M_{7B}	10/0.54
M_{8A}, M_{8B}	12.85/0.54

Table 2. Bias Values

V_{SL}	1V
I_1	10 µA
V_{GG}	1V

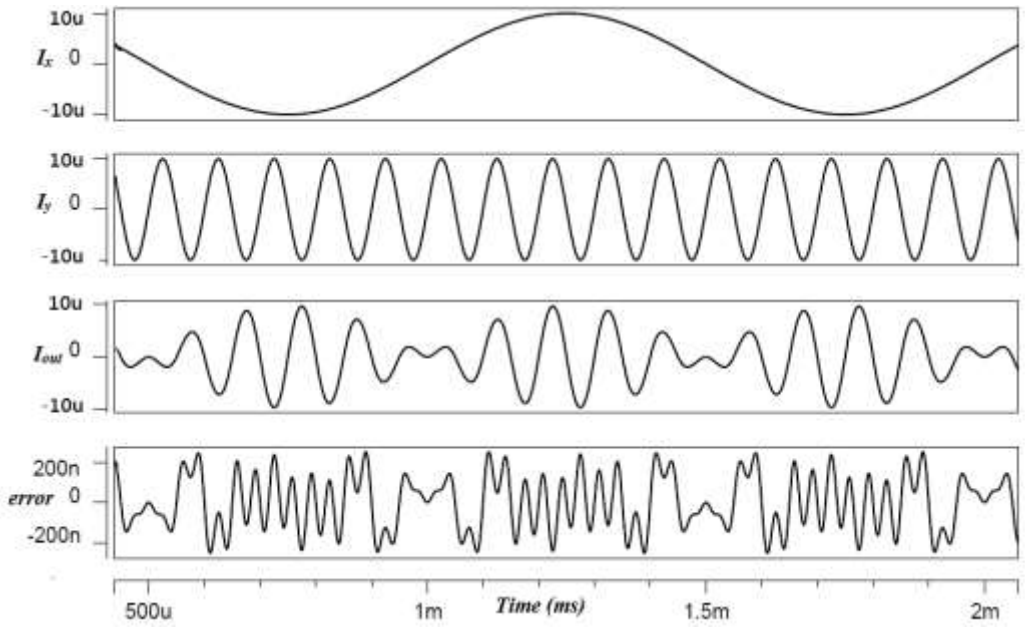

Figure 4. Simulation result of proposed current multiplier circuit and error measurement

The input signals are the sine function with different frequencies of 1 and 10 KHz. As can be seen in Figure 4, the maximum error is less than 2.5%.

Figure 5. proves that change in VSL causes variation on the output current slope.

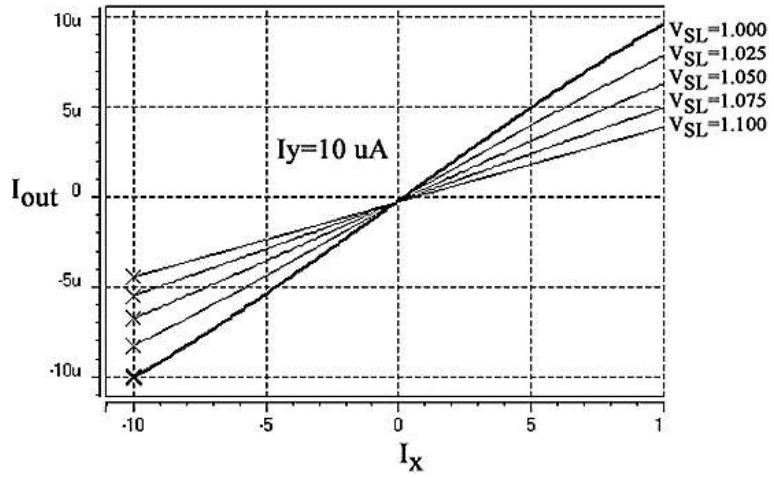

Figure 5. VSL effect on the output current slope

The offset canceled DC transfer function which has the most linear response is shown in Figure 6.

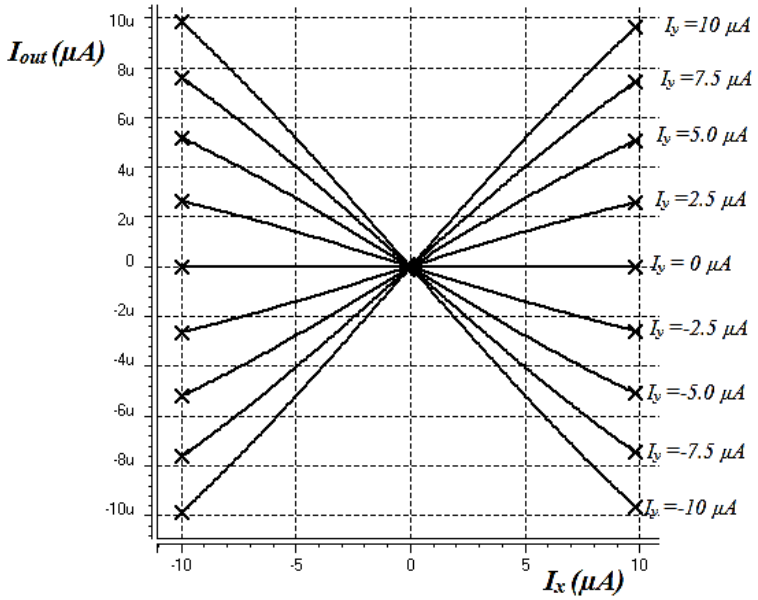

Figure 6. Offset canceled DC transfer characteristics

The Total Harmonic Distortion (THD) versus input current signal at 1 MHz remains far below 1.7% as is shown in Figure 7.

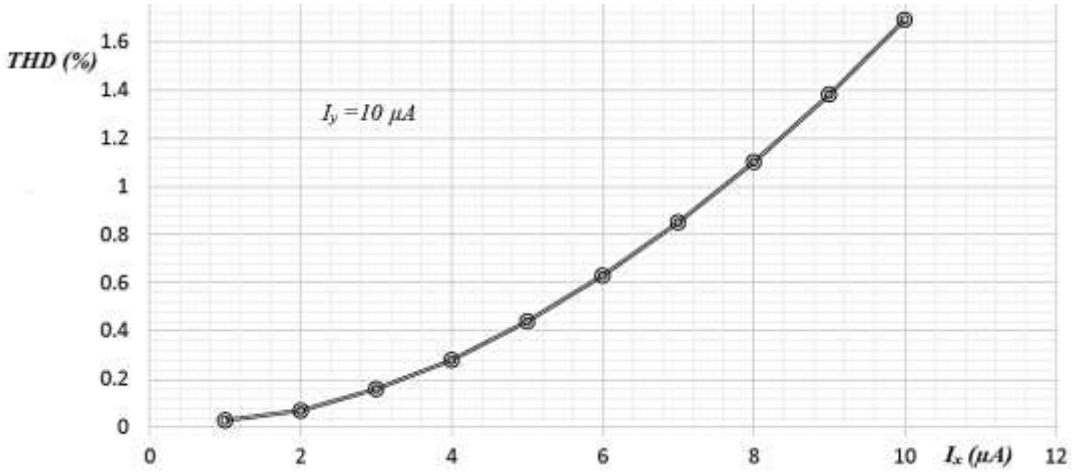

Figure 7. THD(%) variation versus Ix

Table 3. Comparison between this work and other reported papers

Reference	This work	[7]	[2]	[8]	[1]	[9]	[10]	[11]	[12]
Year	2017	2016	2014	2010	2009	2009	2008	2006	2005
F.S* (µm)	*0.18*	0.18	0.35	0.5	0.35	NA	0.35	0.25	0.35
VCC (V)	*1.8*	1.4	±1.5	1.5	3.3	±1.5	3	1.5	2
P_{diss}(µw)	*157*	14.5	475	120	340	1830	3000	NA	5.5
BW (MHz)	*241*	903	24.5	18	41.8	53.1	1	154	0.2
Number of Quadrants	*4*	4	4	2	4	4	4	4	4
THD (%)	*1.77*(1)	0.3	0.87(2)	0.63(3)	0.97	1.39(4)	1(5)	0.25(6)	0.9
Output Current Offset** (nA)	*<1*	10	50	NA	100	NA	80	NA	200

(1) f=1 MHz at 100% bias, 10 µA (2) I_x= 20 µA (3) I_x=50 µA (4) f=100 KHz (5) f=1 KHz (6) f=1 MHz

*** Feature Size**
****The mentioned refrences do not report the exact quantity of this offset; however, this offset can be underestood approximately from DC transfer characteristics figure**

4- Conclusion

In this brief, a four quadrant CMOS current-mode multiplier circuit was proposed. The performance of the multiplier has been simulated using HSPICE software. The advantages of the proposed analog multiplier circuit are high speed, low power consumption and removed dc offset. These distinct achievements and improvements makes the proposed schematic appropriate for very precise and high bandwidth applications.

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